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# PLATO: the status of the Instrument Control Unit following the Critical Design Review

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## ABSTRACT

PLATO (PLAnetary Transits and Oscillations of stars) is the third medium-class mission (M3), selected by the European Space Agency (ESA) in 2014 and adopted in 2017 for the Cosmic Vision 2015-2025 scientific program. The launch is scheduled in 2026 from the French Guiana (Kourou) for a nominal in-orbit lifetime of 4 years plus up to 4 years of possible extension. The main purpose of the mission is the discovery and preliminary characterization of many different types of exoplanets down to rocky terrestrial planets orbiting around bright solar-type stars.

The PLATO spacecraft will operate from a halo orbit around L2 (the Sun-Earth 2nd Lagrangian Point), a virtual point in space, 1.5 million km beyond Earth as seen from the Sun and its Payload will consist of 26 small telescopes (24 normal and 2 fast), pointing at the same target stars, that provide images every 25 seconds with the normal camera and every 2.5 seconds for the two fast cameras, operating in a close loop with the AOCS (S/C Attitude and Orbit Control System). Each camera (consisting of a telescope, the Focal Plane Assembly and its Front-End Electronics) will host four CCDs producing 20.3 megapixels images adding up to 81.4 megapixels per normal camera and 2.11 gigapixels for the overall Payload (P/L). This huge amount of data cannot be transmitted to the ground and need to be processed on-board by the P/L Data Processing System (DPS) made up of various processing electronic units. The DPS of the PLATO instrument comprises the Normal and Fast DPUs (Data Processing Units) and a single ICU (Instrument Control Unit), in charge of HW and SW lossless data compression and managing the P/L through a SpaceWire (SpW) network.

In this paper we will review the status of the Instrument Control Unit (ICU) after its Critical Design Review (CDR) process, performed by ESA and PMC (PLATO Mission Consortium), the results of the performance test preliminary run on the Engineering Model (EM), waiting for the following Engineering and Qualification Model (EQM) and Proto-Flight Model (PFM), and the status of the early models development (Engineering Models 1 and 2, Mass and Thermal Dummy - MTD) that, along with the Boot SW (BSW) burning in PROM readiness, will enable the EQM manufacturing.

(Ref. 1–9).

**Keywords:** Exoplanets,Transit photometry, Large survey, Data Processing System, Instrument Control Unit, Space Mission

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# 1. THE PLATO MISSION

PLATO aims at finding and characterizing a large number of extra solar planetary systems, with emphasis on the properties of the terrestrial planets in the habitable zone around bright solar-like stars. PLATO also aims at investigating seismic activity in stars, enabling the precise characterization of the planets' host star, including its age. It will determine, with unprecedented accuracy, the planet radii, stellar irradiation, architecture of planetary systems and evolutionary ages/stages. In combination with a follow-up based on ground-based observations, and thanks to the brightness of its targets, PLATO will provide accurate planetary masses and mean densities. Moreover, thanks to the asteroseismology observations of a large number of different types of stars, it will significantly contribute to the advancement of stellar interior and evolution models.

PLATO will also carry out an extensive complementary science program that will address a broad range of astronomy topics.

In order to achieve its science objectives, PLATO relies on high-precision photometry to produce a large sample of accurate stellar light curves, obtained over time intervals of months to several years, with a high duty cycle. The planet transit signal and the parent star oscillations are both derived from analysis of the light curve, enabling the detection of transiting planets, the determination of their radii and orbital parameters, and the characterization of their host star.

## 1.1 Spacecraft Architecture

The PLATO Mission is based on a satellite operated by the usual ESA infrastructure and structures in place for Science missions. The Space Segment, also called the Spacecraft for PLATO, comprises two main elements: the Payload and the Platform. The industrial Prime Contractor, OHB Bremen (GE), is in charge of developing the spacecraft platform, supporting the payload functions and performances, and the fully integrated and tested spacecraft (including payload), to be delivered to ESA.

## 1.2 Payload Description

The scientific payload will be developed and provided in collaboration by a European scientific Consortium (the PLATO Mission Consortium - PMC) and ESA. It consists of 26 Cameras that are located in their focal planes and the Data Processing System (DPS), which is the associated digital and analogue electronics.

The DPS is designed to provide control, synchronization and telemetry acquisition to and from the 26 camera units and it manages the interface with the spacecraft service module.

The payload consists of 24 'normal' cameras (N-CAM) with full-frame CCD-based focal planes. They will be read out with a cadence of 25 s and will monitor stars with $mV > 8$. Two additional 'fast' cameras (F-CAM), with high read-out cadence (2.5 s) exploiting frame-transfer CCDs, will be used for stars with mV  4–8.

The 24 Normal Cameras are arranged in four sub-groups of 6 Cameras. All 6 Cameras of each sub-group have exactly the same Field of View (FOV), and the Line Of Sight (LOS) of the four sub-groups are tilted from the payload mean LOS, along which the two Fast Cameras are point. This particular configuration allows surveying a very large field, with parts of the field monitored by 24, 18, 12 or 6 Normal Cameras. This strategy optimizes both the number of targets observed at a given noise level and their brightness.

The assembly of a single Telescope Optical Unit (TOU) and a CCD Focal Plane Array (FPA) is comprised of 4 CCDs and defines each camera. The CCDs work in full frame mode for the Normal Cameras and in frame transfer mode for the Fast Cameras. Each FPA is associated to a Front-End Electronics (FEE), which drives the readout process. The FEEs are interfaced to the Data Processing Unit (DPU). There is one N-DPU per two Normal Cameras, and one F-DPU per Fast Camera. They perform the basic photometric tasks and deliver to DPS light curves, centroid and imagettes[*] captured by the Cameras.

To limit the number of mechanical envelopes, the Normal and Fast-DPUs are grouped in boxes called "Main Electronics Unit" (MEU) and "Fast Electronics Unit" (FEU), respectively. The MEU regroups the N-DPU boards (6x) used for twelve Normal Cameras plus a SpW router and a power supply unit, whereas the FEU regroups the two F-DPUs and two power converters (one for each F-DPU).

[*]CCD area of n x n pixels, surrounding a star of interest, with n = 6, 9, 12

After processing, the science data from each N/F-DPU is downloaded to a central Instrument Control Unit (ICU), which stacks and compresses the data, then transmits them to the Service Module (SVM) for downlink. Data from all individual telescopes are transmitted to the ground, where final instrumental corrections, such as jitter correction, are performed. The F-DPUs will also deliver a periodic pointing error signal to the SVM for the AOCS purposes.

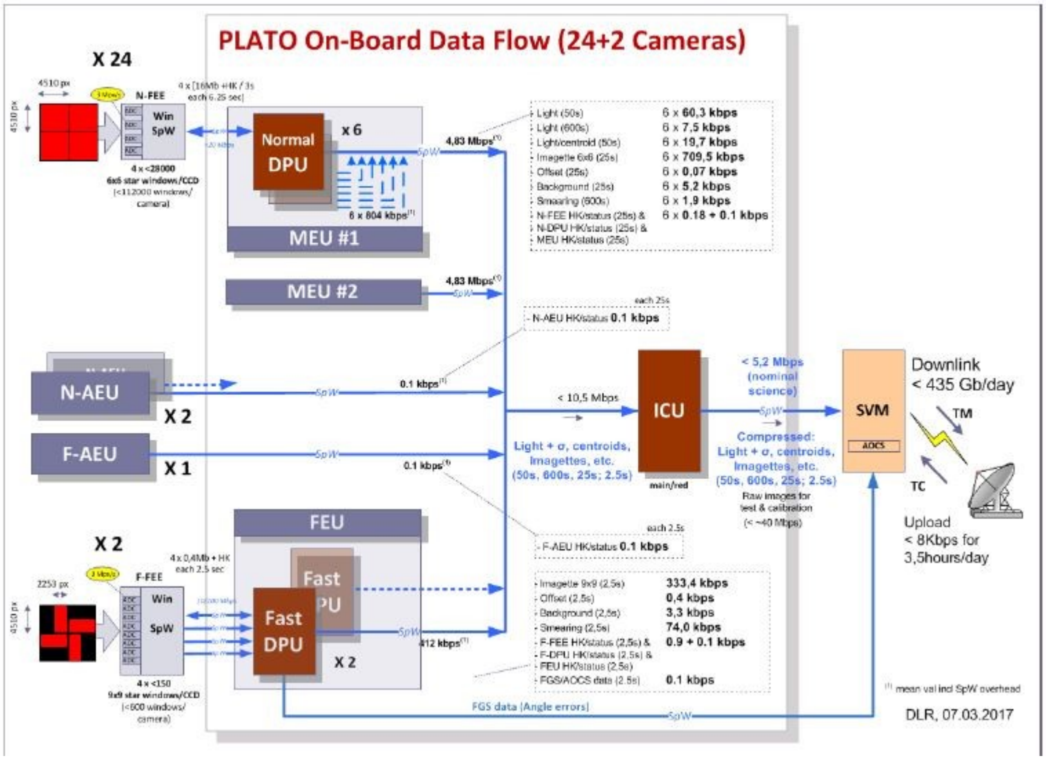


Figure 1. PLATO on board average data flow

## 1.3 The DPS subsystem

The Data Processing Unit (DPU) board is the subsystem in charge of the basic photometric tasks and deliver light curves, centroid curves and imagettes captured by the cameras. There is one N-DPU for 2x N-cameras and one F-DPU for each F-camera (with a total of 12 N-DPUs and 2 F-DPUs).

The Main Electronics Unit (MEU) consists in two boxes (MEU#1 and MEU#2) containing 6 N-DPUs and one power converter each plus two SpW Roouters.

The Fast Electronics Unit (FEU) contains the 2 F-DPUs and two power converters and delivers the periodic pointing error signal from the Fine Guidance Sensor (FGS) to the SVM for AOCS.

The Instrument Control Unit (ICU), which is the subject of this paper, stacks and compresses the data with a lossless algorithm implemented both in HW (for the imagettes) and in SW (for the other Science products) and transmit them to the SVM for downlinking to ground.

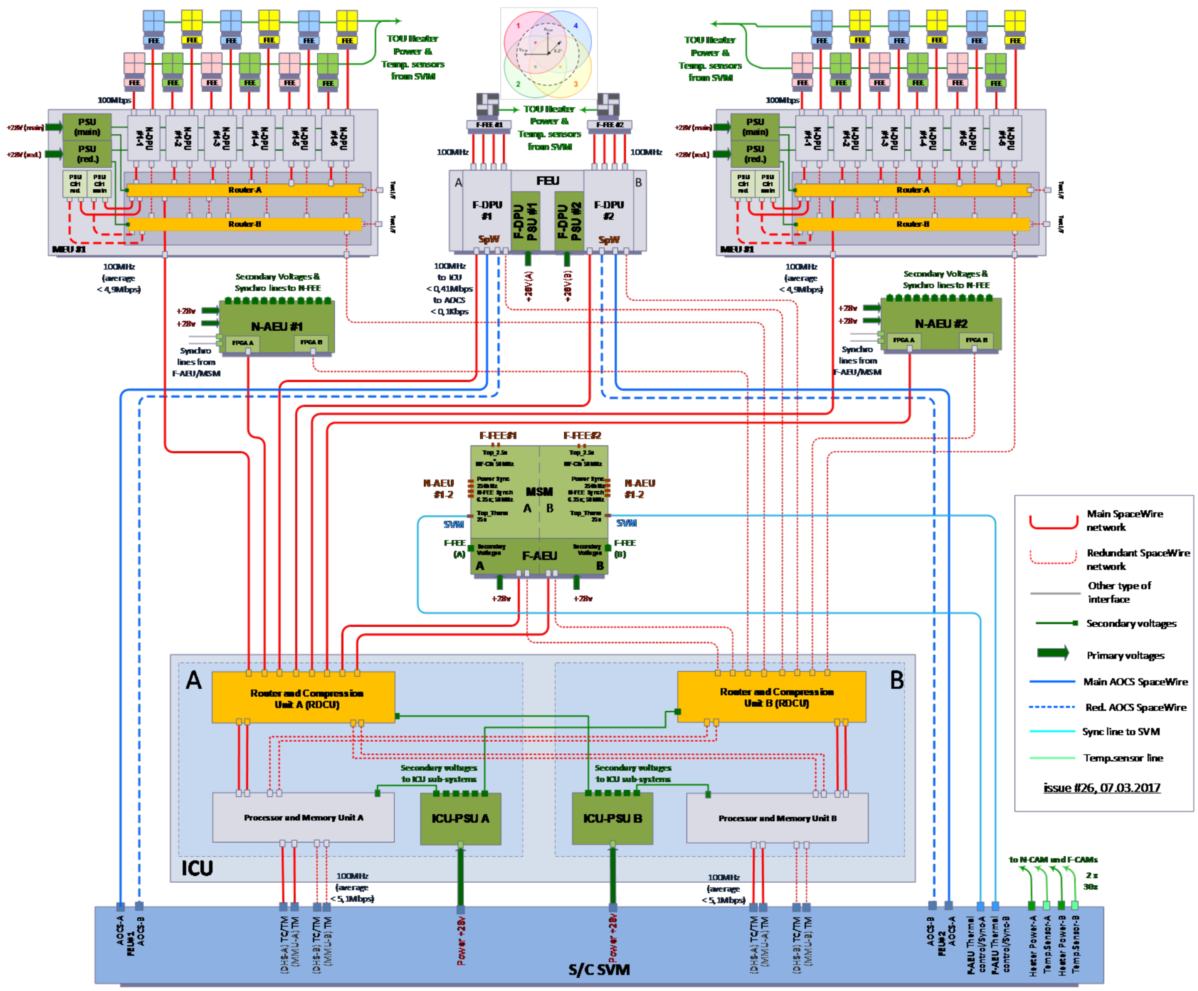


Figure 2. PLATO DPS architecture

## 2. ICU ARCHITECTURE

The ICU is an integrated box with two chains (nominal, N, and cold redundant, R, made up of a CPU/MMU and a PSU board) which can work independently or with a crossed configuration w.r.t. its Router and Data Compression Unit (RDCU) board (N&R).

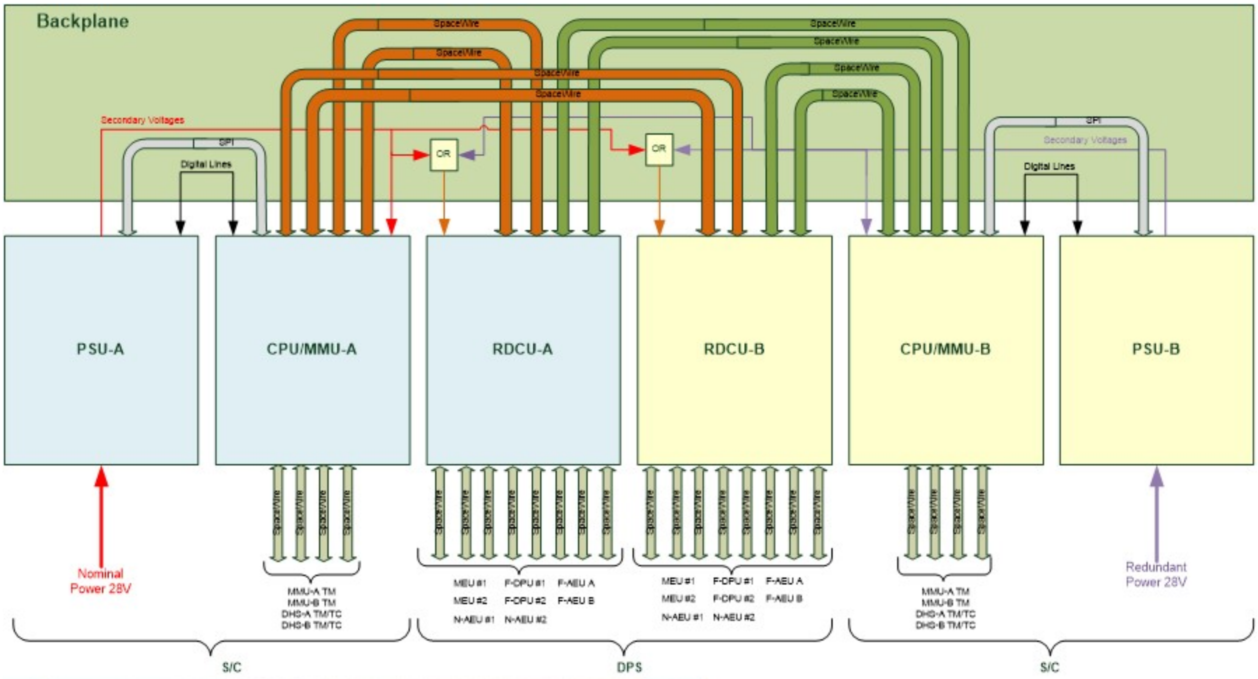


Figure 3. ICU architecture showing its N&R boards and the internal RDCUs N&R cross-strapping

## 2.1 ICU Functions

The PLATO ICU provides the following functions:

- Manage the communication with the spacecraft Service Module (SVM) through a SpW link
- Manage the payload commanding, configuration and monitoring through a SpW link and the DPS SpW network
- Provide mode and status information of the ICU itself and the whole payload
- Collect scientific and housekeeping (HK) data from all cameras
- Compress scientific data before transferring to SVM
- Perform Fault Detection, Isolation and Recovery (FDIR) functions for ICU sub-units, SpW network, SpW routing, DPS units

The ICU supports the start-up and operation sequence of the payload, initiated by the SVM. The following functionalities are provided by the ICU to support the start-up and operation sequence:

- Store and start the ICU boot-software
- Store, load, verify and start of ICU application software
- Establish the SpW link to the SVM after initiation by the SVM
- Send a boot-message to the SVM
- Receive the Telecommands (TCs) from the SVM, execute the TCs or forward the TCs to the DPS subunits
- Synchronize the ICU on-board timer and timers of other units to the SVM on-board-time

- Generate and send ICU HK data to the SVM
- Configure the ICU-router
- Store, load, verify and start the application software on the N-DPUs and the F-DPUs
- Configure the MEU-PSU and the MEU SpW routers
- Initialize/control F-AEU and N-AEUs
- Initialize/control FEU/F-DPU and MEU/N-DPUs
- Request and receive HK data from all other PL units
- Forward HK data from all other PL units
- Command the powering of the Master Synchronization Module (MSM) in the F-AEU
- Command the switch-on of the F-FEEs and N-FEEs secondary power
- Forward the attitude data from the SVM to the FEU
- Process and forward science data from MEUs and FEU
- Store, load and execute payload internal On-Board Control Procedures (OBCPs) dedicated to Instrument independent control w.r.t. the S/C
- Provide the FDIR functionality

The ICU hardware, including its FPGAs FW, BSP (Basic Support Package) and Boot SW (BSW), is designed, developed and manufactured by Kayser Italia contracted by ASI, with contributions from the IWF Space Research Institute from Graz, University of Wien (Austria) and thanks to the overall responsibility by the National Institute for Astrophysics (INAF, Italia), which will also design and deliver the Unit Application SW (ASW).

## 2.2 ICU Hardware description

The ICU is part of the On-Board Data Processing System and consists of the following elements:

- A Power supply Unit (PSU): it receives the 28V from the S/C and provides the secondary supply voltages to the other modules
- A Processor and Mass Memory Unit (CPU/MMU): it is the main data-processing module of the ICU, performing lossless SW compression. It is responsible for payload control and for interfacing the S/C for Telecommands and Telemetries by means of 4 nominal SpW links
- A Router and Data Compressor Unit (RDCU): it implements a SpW router to put in communication the CPU/MMU module with the rest of PLATO DPS and it performs a HW lossless compression (on imagettes only) in order to reach the performance requirements of the ICU
- A Back-Plane (BP): it allows the power distribution and the data sharing between the described Nominal and Redundant modules

## 2.3 ICU Software description

The ICU Software is composed of several different parts:

- ICU Boot SW (BSW) - it is the critical and low complexity software, which is responsible for the maintenance and the boot of the ICU Application Software. For this reason, it has to be carefully developed and extensively tested before the final delivery of the ICU flight model.

  The Boot Software runs after the power-on of the system. In addition to its main function, the BSW implements a series of services tailored to manage the ICU before the Operating System (OS) and ASW boot. BSW is stored in PROM whereas the ICU ASW is stored in MRAM in two copies.

- ICU Application SW (ASW) - it is the software that implements the entire requirements needed to fulfil the PLATO scientific mission. It is also responsible to implement the FDIR procedures for the ICU sub-units, the SpW network, SpW routing and the DPS sub-systems connected by SpW links and routers.

- Software drivers for CPU/MMU HW peripherals to be provided to ASW (the so-called Basic Support Package - BSP).

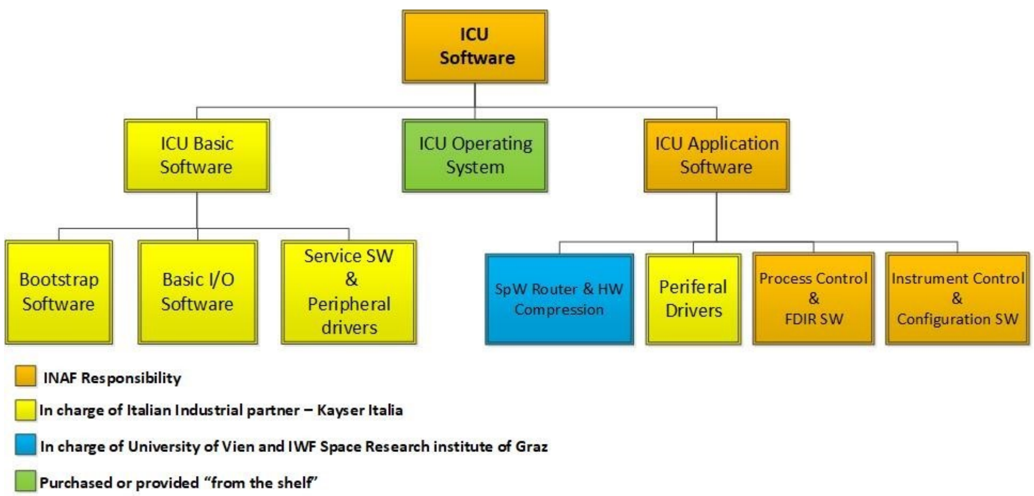


Figure 4. ICU software product tree and partners responsibility

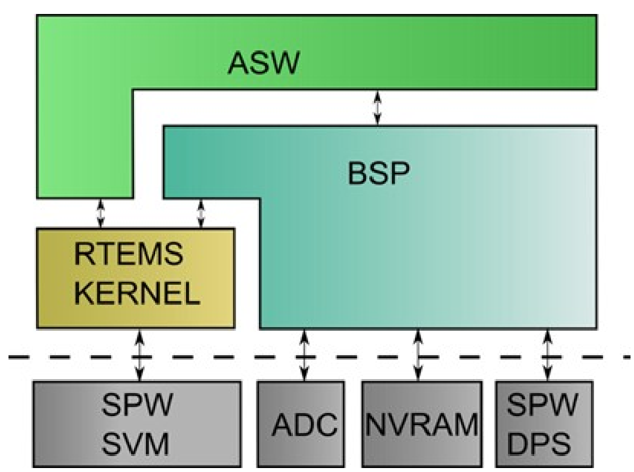


Figure 5. ICU software block diagram

## 2.4 ICU status following the Preliminary Design Review

After the ICU Preliminary Design Review (PDR), two Engineering Models (EM) and one Mass & Thermal Dummy (MTD) model have been built:

- EM#1, without redundancy, to be delivered to the Prime for testing on the spacecraft avionic model
- EM#2, with full redundancy, to be delivered to PMC for DPS-level testing at DLR in Berlin and, then, used for ICU ASW development
- ICU MTD to be used for structural and thermal qualification at spacecraft level

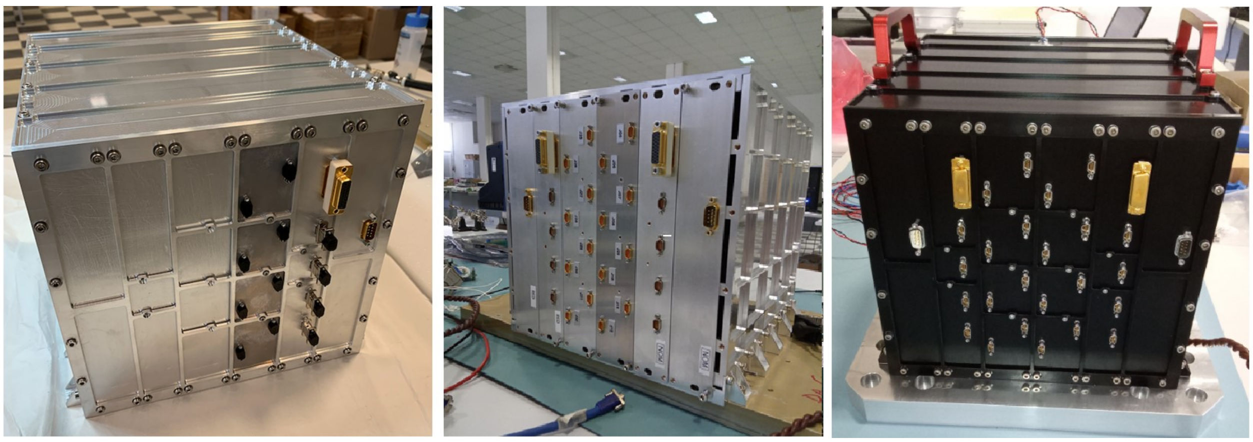

Figure 6. From left to right: picture of the EM#1 (single chain, N), EM#2 (double chain, N and R) and MTD

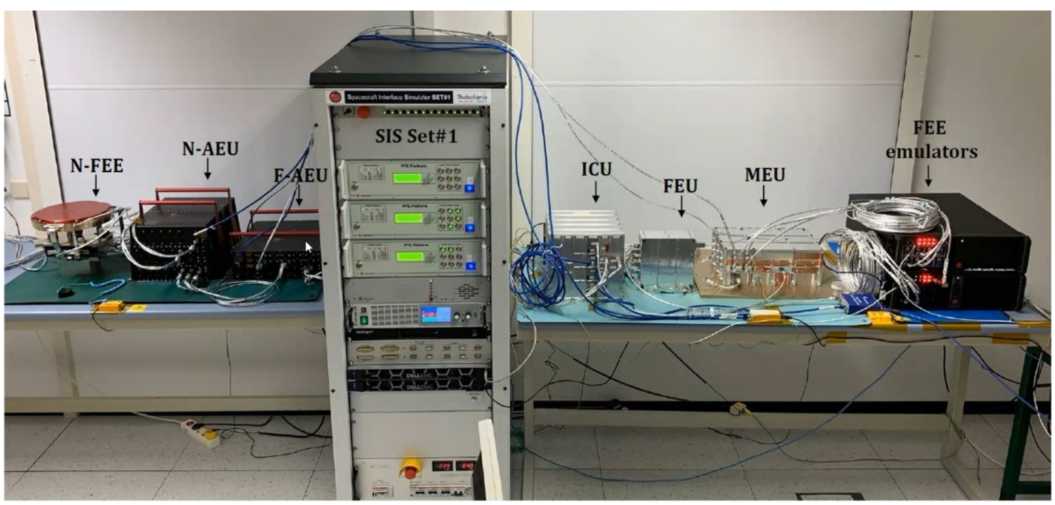


Figure 7. DPS EM Bench test (courtesy DLR, Berlin)

The EMs have been formerly used for integration with the other DPS sbssystems and to perform functional tests at DLR at DPS level in addition to performance tests and software development/test at the ICU team premises. In particcular:

- The ICU EM#1 model has been delivered to PMC (DLR, Berlin) for preliminary DPS level testing and has been integrated and delivered together with the overall DPS EM-grade for the avionic F-Chain level testing and, later on, for Electrical and Functional Model testing at the S/C Prime premises

- The ICU EM#2 model has been shipped to DLR in order to be integrated in the DPS EM Test Bench in Berlin, following the ICU EM#1 shipping to the S/C Prime
- Finally, the MTD was delivered to the Prime and used for structural and thermal qualification at S/C level

## 3. AN OVERVIEW ON THE ICU CRITICAL DESIGN REVIEWS

Following the PDR, five Critical Design Reviews (CDRs) have been foreseen for the ICU subsystems that are considered critical and need to demonstrate a high level of design and testing procedures consolidation. The goal of the CDRs is to verify the readiness of the project to move on into the following phase.

The CDRs for the ICU DPS subsystem are listed and then described in the following:

1. ICU unit CDR
2. RDCU FPGA CDR
3. DPU/MMU FPGA CDR
4. Boot Software (BSW) CDR
5. Application Software (ASW) CDR

Presently, 1-4 have been successfully run, while 5 is going to be faced.

## 4. UNIT CDR

The Unit CDR focuses on the development of the ICU HW to ensure that its design is fully consolidated, the test programme is designed and complete, specifications and procedure are in place, and all the quality aspects are fully met.

The review is held to authorise the production and assembly of the hardware elements for EQM and the production of the hardware elements for PFM, confirmed by the Manufacturing Readiness Review (MRR).

The specific objectives for the Unit CDR are:

- Confirm that the ICU design meets the applicable functional and performance requirements, supported by analyses and/or tests
- Verify the robustness of the ICU design, and its compliance to the allocated resources, margins required at CDR, design, interface and product assurance requirements
- Confirm the completeness of the definition of the external hardware and software interfaces and their formalization in Interface Control Documents (ICDs)
- Confirm the maturity and feasibility of the ICU verification and qualification plans, including on-ground calibration and characterization plans, and their ability to demonstrate compliance with all requirements
- Verify the approval status of declared parts, materials, processes and components and their qualification status
- Confirm the completeness of all test specifications and the maturity of relevant test procedures
- Verify the maturity of the verification, traceability and compliance matrices and the adequate approval of any relevant deviations and/or waivers
- Verify the completeness of the schedule, its margins and contingencies and its overall compliance with the need dates at Camera/DPS level

- Verify the completeness of the risks register, and the adequacy of the mitigation plans and actions
- Confirm the completeness of the documentation for tracking, handling, transportation, operation, and maintenance of the ICU

The Unit CDR started on March 2021 with the "Readiness check-out" review and ended in November 2021 with a successful "Board meeting", enabling the production and assembly of the hardware elements for the EQM model, pending some further verifications at BSW (i.e. the Independent SW Validation and Verification - ISVV by a third party) and BSP/ASW level.

# 5. FPGA CDR

The general objectives of the Unit FPGAs CDR are as follows:

- Verification of the actual implementation of the FPGA Control Plan, Development Plan and Verification Plan, by means of inspections and reviews
- Assessment of the quality and of the completeness of the provided documentation
- Verification that the configuration management system is properly defined and used.
- Suitability of workarounds put in place of encountered problems with design tools
- Verification that all inputs to the design and all automatically generated data being necessary to reproduce the design - such as simulation pattern, schematics, VHDL source codes, compiler software version, conversion parameter settings, manufacturer libraries, synthesis scripts etc – are put under configuration control and safely stored and preserved

## 5.1 CPU/MMU FPGA CDR

The purpose of the CPU/MMU FPGA CDR was to formally approve the design, layout and the release for of the programming of the device used for the validation phase, here before EQM assembly. The CPU/MMU FPGA device is based on the RTAX FPGA family from Microsemi. The chip is used to extend the communication features between the CPU/MMU and the RDCU boards, handling SpW interfaces, SDRAM buffering and data flow control.

The CPU/MMU FPGA is located on the ICU processor board and performs the following functions:

- PCI interface management to the ICU processor
- SpW RMAP interface management towards the MEU, FEU and AEUs
- PUS packet management
- Interface management to the SDRAM banks managed by the FPGA[†]

The DPU FPGA CDR started on March 2021 with the "Readiness check-out" review and ended in November 2021 with the "Board meeting", which was declared successful and the following authorization for the design, production and assembly of the FW and hardware elements for the EQM model, was granted.

[†] part of the SDRAM on-board memory (512 MB over 1 GB) is managed by the CPU

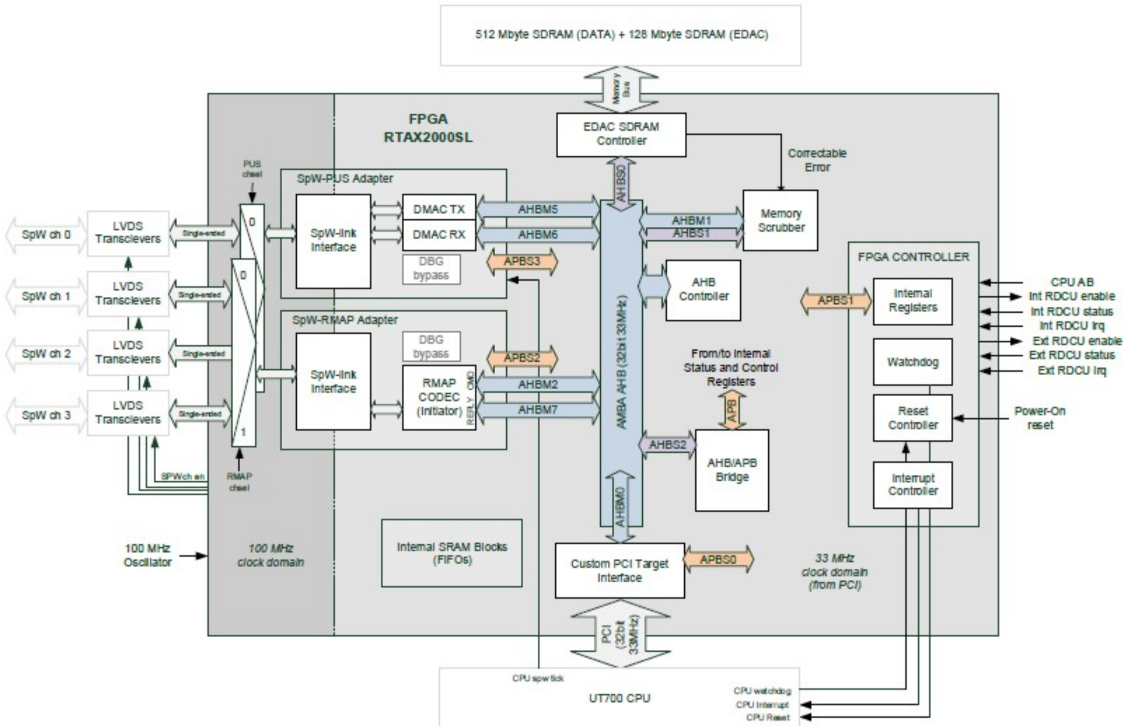

Figure 8. CPU/MMU FPGA architecture

## 5.2 RDCU FPGA CDR

The purpose of the RDCU FPGA CDR was, as for the CPU/MMU FPGA, to formally approve the design and layout and the release for of the programming of the device used for the validation phase, here before EQM assembly.

The RDCU FPGA device is based on a RTAX2000 FPGA which is used to implement the hardware data compressor functionality. It provides access to the RDCU on-board SRAM memory for data storage (size 8 MByte) and the control registers via the RMAP protocol. The logic also collects the housekeeping and link status values, which also can be read back via RMAP.

The RDCU FPGA is located on the RDCU board (compression and ICU SpW rouuting module) and performs the following functions:

- SpW RMAP interface management to the ICU processor board
- Lossless compression of the incoming data (imagettes) from the DPUs

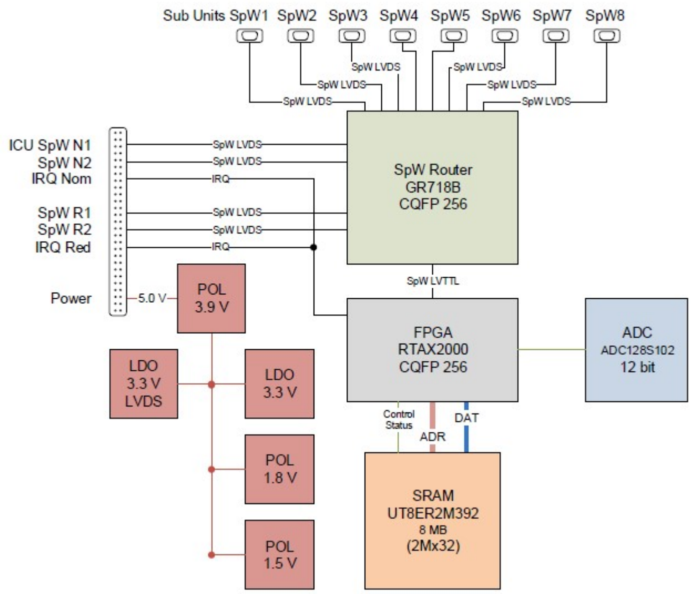


Figure 9. RDCU electrical block diagram (courtesy IWF, Graz)

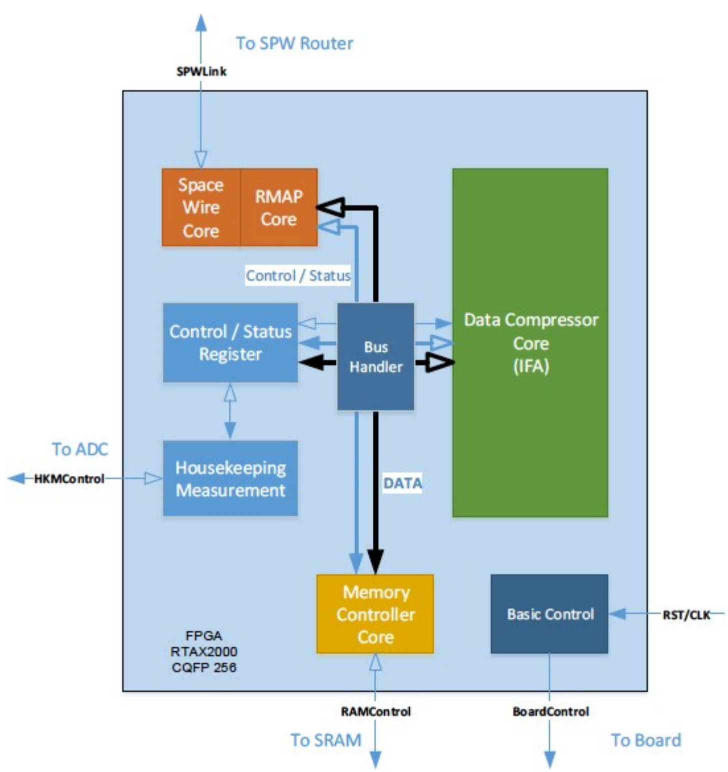


Figure 10. RDCU FPGA internal block diagram (courtesy IWF, Graz)

The RDCU FPGA CDR started on March 2021 with the "Readiness check-out" review and ended in July 2021 with the "Board meeting", which was declared successful and the following phase, the production and assembly of the RDCU boards for the ICU EQM model was started.

## 6. BOOT SOFTWARE CDR

The ICU Boot Software (BSW), and BSW in general, is classified as an ECSS "Category B" software with a higher criticality w.r.t. the Unit Application Software, as it is in charge of the ICU and overall instrument booting and it is finally burned into the PROM on each of the two DPU CPU/MMU modules (N and R) of the ICU. It is the only Category B SW hosted by the Instrument and so the most critical.

The Boot SW is in charge of the following functions:

- Initialize the CPU/MMU HW
- Initialize the communication with the Spacecraft
- Check of the integrity of the hardware (check of the memories)
- Manage Internal Housekeeping (HK) data
- Manage dedicated Telecommands and Telemetries
- Waiting for Telecommands either to launch the ASW or to upload a new ASW image
- Start the ASW (comprehensive of the RTEMS OS)

The purpose of the BSW CDR is to formally approve its design and code to be released for the validation phase, before the EQM assembly process, and its main goals are:

- To verify that the developed software tasks composing the BSW have been successfully integrated and the software validation is performed
- To assess that the Independent SW Validation and Verification (ISVV) process by a third party has been performed
- To demonstrate that the Boot Software is ready for qualification on the EQM hardware burned in PROM

The BSW CDR followed both the ICU hardware and FPGAs CDRs. It started on March 2021 with the "Readiness check-out" review and finished in November 2021 with the "Board meeting". The BSW CDR was declared successful, pending for the completion of some actions and the completion of the ISVV on the BSW. The following phase, concerning the BSW burning in PROM, will be accomplished after the EQM MRR.

## 7. APPLICATION SOFTWARE CDR

The Application Software, including the BSP (Basic Support Package), is a Category C software (lower criticality w.r.t. the BSW) and starts its operations once the BSW has completed its activities. The ASW has the following functions:

- Acceptance of instrument commands from the Service Module (SVM)
- Execution of predefined instrument command sequences
- Instrument health/status monitoring
- Implementation of pre-defined procedures on detection of instrument anomalies: the instrument shall be able to adjust parameters and/or switch operating mode and/or activate subsystem redundancy when an anomaly occurs
- HK data acquisition and packetization
- Science data acquisition, compression and packetization

- Transmission of data (HK, events and TC verification) from the instrument to SVM-DHS (Data Handling System)
- Transmission of science data to the SVM-MMU (Mass Memory Unit)
- Handling of the DPUs boot process
- Handling of DPUs images (storing, uploading and patching)
- Handling of time code and time distribution to sub-systems
- Setup of the Payload SpW network through uploadable tables
- Ability to load, via TCs, replacement and/or additional SW (patches, tables, etc)
- Possibility to load and dump part of DPS system memory also through RMAP protocol
- Possibility to write and check the Non-Volatile Memory (NVM, a MRAM type memory): possibility to inhibit these functions during flight operations

The main purpose of the ASW CDR is to:

- Formally approve the completion of the v0.8 Application Software Verification & Validation program
- Formally approve the v1.0 Application Software design and code to be released for the validation phase
- Formally approve the validation of the BSP against the HW-SW ICD

The preliminary activities concerning the ASW CDR review are presently ongoing in order to fulfil the selected precondition for the review. The date for the "Readiness check-out" will be established as soon as the results of the ASW full functional and performance test (FFPT) will be completed and the relevant report will be delivered to PMC.

### 7.1 Preliminary performance test

The aim of the ICU lossless data compression performance verification (on imagettess HW compression only, performed by RDCU exchanging data with the ICU processor) is to verify that the chain RDCU-ICU-Compressor-ICU-SVM is able to cope with the PLATO science requirements (total number of imagettes, compression ratio, data rate, etc.). Since it was not possible to execute a test with 24 N-CAMs, a preliminary trend analysis has been conducted by using 6 N-CAMs generating reference data to verify that a sufficient margin is available for the nominal configuration.

Considering that in 25s, data from 24 cameras have to be compressed, an optimum average total duration compression for one frame per camera is 1.04s. Therefore, for a couple of frames, each camera should complete the compression activity within 2.08s.

The preliminary performance test was conducted by simulating a scenario with:

- 1 Single N-CAM (1.98 MB / 25s)
- 2 N-CAMs generating data in parallel (3.96 MB / 25s)
- 6 N-CAMs generating data in parallel (11.88 MB / 25s)

To verify that also with 24 cameras there is sufficient margin for the imagettes HW compression activity, we considered the estimated compression time needed for two cameras, 6 cameras and 24 cameras as well. The estimated time has been calculated as the total time to compress two frames when only one camera is used, multiplied by the number of cameras. The measured average total duration to compress 2 frames with data from a single camera is about 1.85s, lower than the requested value, with 11% margin.

This results theoretically show that the HW compression performance specification is achievable. To confirm this preliminary results a full test with 24 cameras is scheduled for the next months, whose outcome will be presented in a dedicated technical report.

## 8. CONCLUSION

The CDR reviews of the ICU are almost completed, except the one concerning the ASW that will be faced during the next months. The three CDR reviews concerning the ICU hosted hardware and firmware (Unit HW, CPU/MMU FPGA and RDCU FPGA) were declared successful and provided the authorization for the production and assembly of the hardware elements for the EQM model.

The BSW CDR was declared successful, pending the completion and closure of some action items and the completion of the ISVV. The BSW burning in PROM will be done soon after the EQM Manufacturing Readiness Review granting by PMC.

The formal approval of the ASW readiness and verification program against the SW requirements specification (SRS document flown down from the SW System Specification document) and of the BSP testing and verification program against the HW-SW ICD will be completed until the end of the ASW CDR.

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Members of the PLATO Consortium can be found at https://platomission.com/.

The ESA PLATO mission website is https://www.cosmos.esa.int/plato. We thank the teams working for PLATO for all their work.

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